Notice of Allowability	Application No.	Applicant(s)	
	10/708,380	HUISMAN ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt filed on 05/21/07*.

2. ☒ The allowed claim(s) is/are *1-9, 11-22 and 24-32 (reunmbered as 1-30)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *07/20/07* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

7/20/2007

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and or additions be acceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no latter than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steven M. Santisi on 07/20/07.

2. The application has been amended as follows:

Cancel claim 10.

Cancel claim 23.

Replace Claim 8:

8. (Currently amended) A method of testing and diagnosing a scan chain comprising:

altering the function of a scan chain flush test mode of one or more of a plurality of latches included in the scan chain;

and employing the flush test mode to test and diagnose the scan chain.

With

8. (Currently amended) A method of testing and diagnosing a scan chain comprising:

altering the function of a scan chain flush test mode of one or more of a plurality of latches included in the scan chain wherein altering the function of the scan chain flush test mode includes altering the function of the scan chain flush test mode such that an alternating set of complementing states are propagated through the scan chain; and

employing the flush test mode to test and diagnose the scan chain.

Replace claim 21:

21. (Currently amended) An integrated circuit (IC) for testing and diagnosing a scan chain comprising:

a plurality of latches catenated into the scan chain; and one or more logic devices coupled to the scan chain;

wherein the IC is ~~adapted~~ configured to: alter the function of the scan chain flush test mode;

and employ the flush test mode to test and diagnose the scan chain.

With

21. (Currently amended) An integrated circuit (IC) for testing and diagnosing a scan chain comprising:

a plurality of latches catenated into the scan chain;

and one or more logic devices coupled to the scan chain; wherein the IC is ~~adapted~~ configured to:

alter the function of the scan chain flush test mode such that an alternating set of complementing states are propagated through the scan chain;

and employ the flush test mode to test and diagnose the scan chain.

Examiner's statement for reason for allowance

3. Claims **1-9 and 11-22 and 24-32** have been allowed.

As per claim 1:

The prior art of record, Barnes (U.S. PN: 6,622,273) teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45).

The prior art or record, (U.S. PN: 4,945,536) Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation

characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious operating the one or more latches whose first test modes are modified in the modified first test mode; and operating one or more of the plurality of latches included in the scan chain in a second test mode wherein adjacent portions of a non-defective section of the scan chain store complementary signals. Consequently, claim 1 is allowed over the prior art.

Claims **2-6,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 7:

The prior art of record, Barnes (U.S. PN: 6,622,273) teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). The prior art or record, (U.S. PN: 4,945,536) Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious operating the one or more latches whose first test modes are modified in the modified first test mode to store a first set of data in the scan chain, operating one or more of the plurality of latches included in the scan chain in a second test mode to output the first set of data, while inputting a second value to the scan chain, operating the one or more latches whose first test modes are modified in the modified first test mode to store a second set of data in the scan chain, operating one or more of the plurality of latches included in the scan chain in the second test mode to output the second set of data and employing the first set of data and the second set of data to isolate a defect in the scan chain. Consequently, claim 7 is allowed over the prior art.

Claim **28,** which is/are directly or indirectly dependent/s of claim 7 is also allowable over the prior art of record.

As per claim 8:

The prior art of record, Barnes (U.S. PN: 6,622,273) teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). The prior art or record, (U.S. PN: 4,945,536) Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain

test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious altering the function of a scan chain flush test mode of one or more of a plurality of latches included in the scan chain wherein altering the function of the scan chain flush test mode includes altering the function of the scan chain flush test mode such that an alternating set of complementing states are propagated through the scan chain and employing the flush test mode to test and diagnose the scan chain Consequently, claim 8 is allowed over the prior art.

Claims **9, 11 and 29,** which is/are directly or indirectly dependent/s of claim 8 are also allowable over the prior art of record.

As per claim 12:

The prior art of record, Barnes (U.S. PN: 6,622,273) teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). The prior art or record, (U.S. PN: 4,945,536) Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation

characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious one or more logic devices coupled to the plurality of latches included in the scan chain, wherein the IC is configured ~~adapted~~ to modify a first test mode of one or more of the plurality of latches included in the scan chain, operate the one or more latches whose first test mode are modified in the modified first test mode, and operate one or more of the plurality of latches included in the scan chain in a second test mode wherein adjacent portions of a non-defective section of the scan chain store complementary signals. Consequently, claim 12 is allowed over the prior art.

Claims **13-19 and 30,** which is/are directly or indirectly dependent/s of claim 12 are also allowable over the prior art of record.

As per claim 20:

The prior art of record, Barnes (U.S. PN: 6,622,273) teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). The prior art or record, (U.S. PN: 4,945,536) Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation

characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious one or more logic devices coupled to the plurality of latches included in the scan chain, wherein the IC is configured to modify a first test mode of one or more of a plurality of latches included in the scan chain, while inputting a first value to the scan chain, operate the one or more latches whose first test modes are modified in the modified first test mode to store a first set of data in the scan chain, operate one or more of the plurality of latches included in the scan chain in a second test mode to output the first set of data, while inputting a second value to the scan chain, operate the one or more latches whose first test modes are modified in the modified first test mode chain to store a second set of data in the scan chain, operate one or more of the plurality of latches included in the scan chain in the second test mode to output the second set of data, and employ the first set of data and the second set of data to isolate a defect in the scan chain. Consequently, claim 20 is allowed over the prior art.

Claims **31,** which is/are directly or indirectly dependent/s of claim 20 is also allowable over the prior art of record.

As per claim 21:

The prior art of record, Barnes (U.S. PN: 6,622,273) teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see

col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). The prior art or record, (U.S. PN: 4,945,536) Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62).

However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious one or more logic devices coupled to the scan chain, wherein the IC is configured to alter the function of the scan chain flush test mode wherein the IC is further configured to alter the function of the scan chain flush test mode such that an alternating set of complementing states are propagated through the scan chain and employ the flush test mode to test and diagnose the scan chain. Consequently, claim 21 is allowed over the prior art. Consequently, claim 21 is allowed over the prior art.

Claims **22-26 and 32,** which is/are directly or indirectly dependent/s of claim 21 is also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Esaw T. Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8am-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Esaw Abraham

Esaw Abraham

Art unit: 2112

GUY LAMARRE
PRIMARY EXAMINER